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VLSI Design Technologies for Future Network

～ A High-speed Packet-filter with Mismatch-detection Circuit～

NTT

Motivation

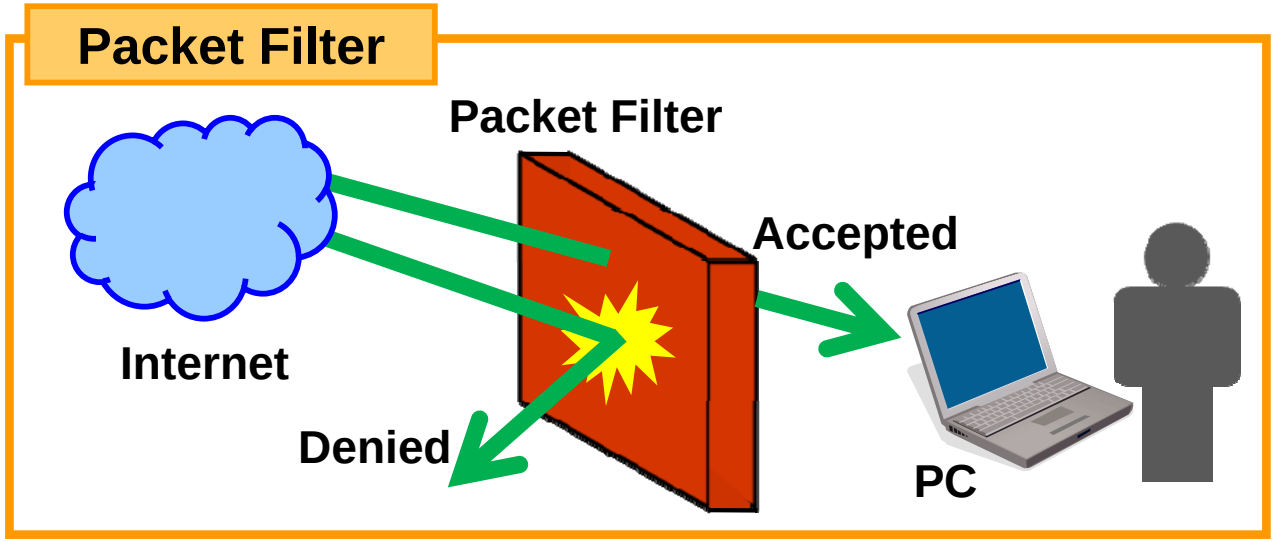
Our goal is to speed up communications circuits for the future network. Communications devices generally contain a packet filter for filtering received packets. The filter becomes a bottleneck in speeding up communications devices because it has to match a received packet with one of many registered filter conditions. So, we focus especially on speeding up the packet filter.

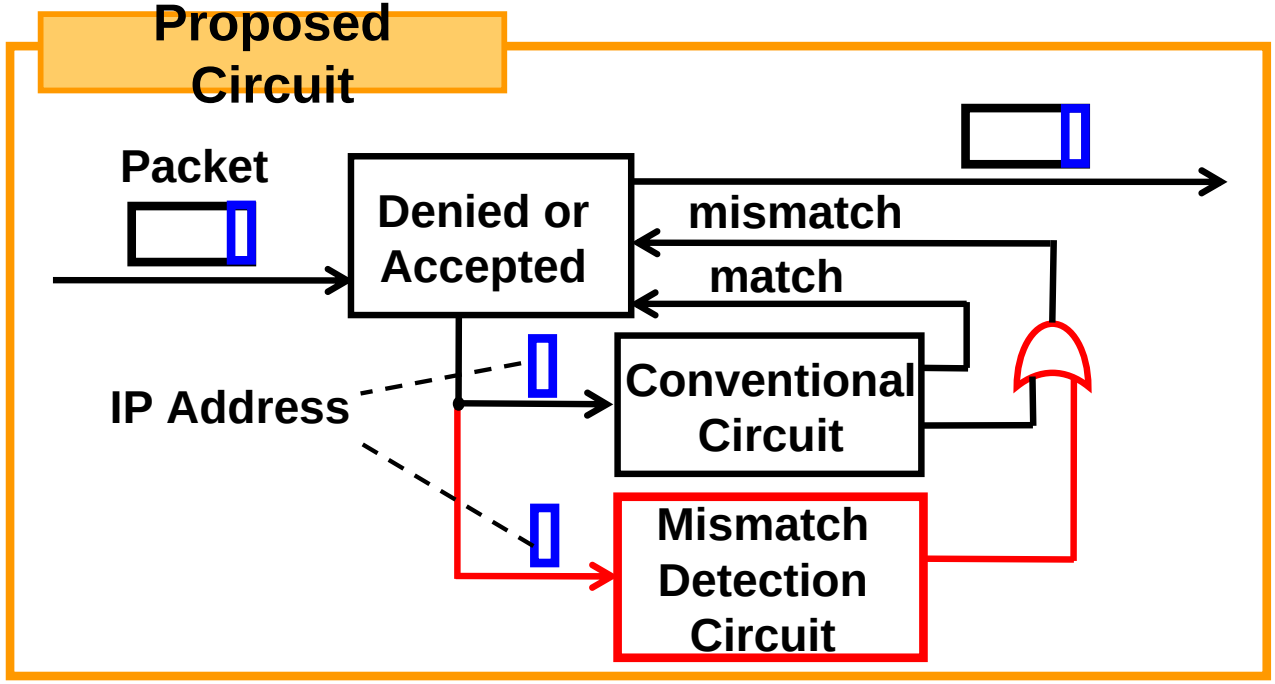
Originality

A conventional packet filter declares a match when it finds the same condition as the received packet and declares a mismatch when it doesn't. The declaration of a mismatch takes a longer. To shorten this time, we propose a packet filter with a mismatch detection circuit. The mismatch detection circuit is added to the conventional one. The proposed circuit enables a packet filter to quickly declare whether the received packet matches the condition or not. Using the mismatch detection circuit, we have increased the speed of the packet filter.

Impact

The proposed packet filter helps communications devices communicate faster. Internet users will therefore be able to download or upload large files in a shorter time and enjoy internet service like IP-TV comfortably.





NTT Microsystem Integration Laboratories

Contact: Naoki Miura naoki@aecl.ntt.co.jp