

CMOS FET Comanding Current-Mode Integrator

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Abstract

A new CMOS comanding current-mode integrator is proposed. The comanding integrator is based on MOS TransLinear principle and utilizes a nature of MOSFET square-law. SPICE simulation results demonstrate good performances.

1 Introduction

On-going trend towards lower power supply voltages have resulted in a decrease of the dynamic range of filters designed using conventional circuit techniques. One of the possible solutions is instantaneous comanding (compressing-expanding)[1]–[6] of signal. Using this approach, the capacitance voltage swing will become smaller than the input signal swing. Consequently, the power supply voltage will be less restrictive to the maximal input signal.

The structure of CMOS FET comanding integrator was proposed in [6]. In order to get the comanding integrators, the translinear principle[7] is one of the suitable techniques. A comanding integrator using MOS TransLinear (MTL) principle is proposed in [5]. However it is quite complicated.

In this paper, a simple CMOS FET comanding current-mode integrator is proposed. To compose a compressing characteristic, the MTL principle is employed and the square-law of MOS FET is employed to realize an expanding characteristic. We can reduce the number of FETs by sharing the current of two compressing circuit components. SPICE simulations were performed to verify the proposed circuit.

2 General Principle

Figure 1 shows the block diagram of the proposed comanding integrator. From the figure, we have;

$$\left. \begin{aligned} I_{out} &= f(V_2) \\ V_2 &= K_I \int I_1 dt \\ I_1 &= h(I_{out})I_{in} \end{aligned} \right\} \quad (1)$$

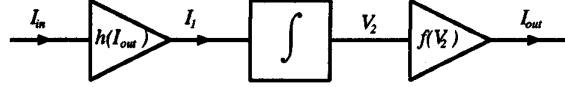


Figure 1: Basic concept of a comanding current-mode integrator

where, $f(V_2)$ is the characteristic of the expanding circuit and is a function of V_2 , $h(I_{out})$ is the gain of the compressing circuit and a function of I_{out} , and K_I a constant of the integrator.

Since we realize a linear integrator with respect to input-output current, we must have the following expression;

$$I_{out} = \alpha \int I_{in} dt \quad (2)$$

where α is a constant. Differentiating Eq. (2), we get

$$\frac{dI_{out}}{dt} = \alpha I_{in}. \quad (3)$$

dI_{out}/dt is rewritten as

$$\begin{aligned} \frac{dI_{out}}{dt} &= \frac{df(V_2)}{dV_2} \cdot \frac{dV_2}{dt} \\ &= \frac{df(V_2)}{dV_2} \cdot K_I I_1 \\ &= \frac{df(V_2)}{dV_2} \cdot K_I h(I_{out}) I_{in}. \end{aligned} \quad (4)$$

From Eqs. (3) and (4), we get

$$K_I h(I_{out}) \cdot \frac{df(V_2)}{dV_2} = \alpha. \quad (5)$$

Now we employ the MOS FET square-law as the expanding function $f(V_2)$. That is,

$$I_{out} = f(V_2) = K(V_2 - V_T)^2. \quad (6)$$

Differentiating Eq. (6), we get,

$$\frac{df(V_2)}{dV_2} = 2K(V_2 - V_T) = 2\sqrt{KI_{out}}. \quad (7)$$

Then from the Eqs. (5) and (7), the compressing function $h(I_{out})$ must be

$$h(I_{out}) = \frac{\alpha}{2K_I\sqrt{K}I_{out}} = \frac{\alpha'}{\sqrt{I_{out}}} \quad (8)$$

where $\alpha' = \frac{\alpha}{2K_I\sqrt{K}}$. In order to realize Eq. (8), one can take advantage of the MTL principle, which will be shown in the next section.

3 Current-Mode Comanding Integrator

3.1 Compressing Circuit

Figure 2 shows a square-root circuit using the MTL principle. The drain current I_b of M17 is given by,

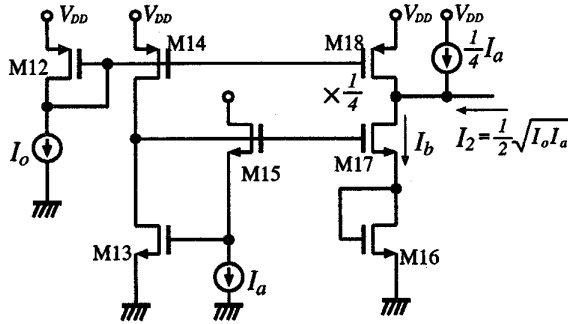


Figure 2: Square-root circuit using translinear principle

$$I_b = \frac{1}{4}(I_a + I_o) + \frac{1}{2}\sqrt{I_a I_o}. \quad (9)$$

The current mirror consisting of M12, M14, and M18, and current source $\frac{1}{4}I_a$ in Fig. 2 subtract the off-set current $\frac{1}{4}(I_a + I_o)$ from Eq. (9) and we get the output current I_2 of Fig. 2 as follows:

$$I_2 = \frac{1}{2}\sqrt{I_a I_o}. \quad (10)$$

We can see from Eq. (10) that I_2 is proportional to the square-root of I_o .

Next, we consider the circuit shown in Fig. 3. The output current I_d of Fig. 3 is expressed as

$$I_d = 2I_2 + \frac{I_c^2}{8I_2}. \quad (11)$$

Then, we can realize $1/I_2$. Finally, in order to eliminate the offset current $2I_2$ and achieve the compressed

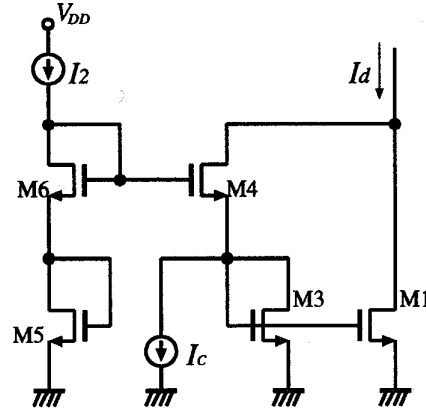


Figure 3: Dividing circuit using translinear principle

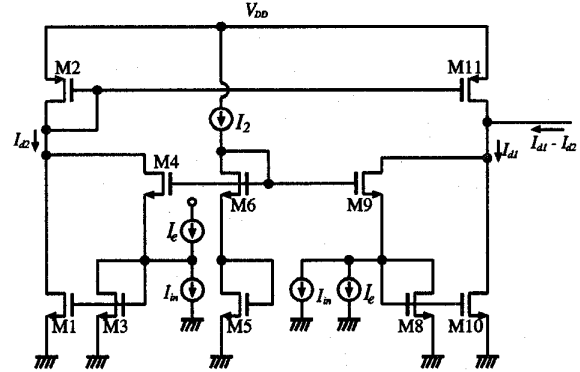


Figure 4: Compression circuit

current $I_1 (= h(I_{out}) \cdot I_{in})$, we propose the compression circuit shown in Fig. 4 which consists of two circuits of Fig. 3. One circuit is fed with the current I_{c1} in place of I_c and another with I_{c2} , where

$$I_{c1} = I_{in} + I_e \quad (12)$$

$$I_{c2} = I_{in} - I_e. \quad (13)$$

thus the output current of each circuit is given by

$$I_{d1} = 2I_2 + \frac{I_{c1}^2}{8I_2} \quad (14)$$

$$I_{d2} = 2I_2 + \frac{I_{c2}^2}{8I_2}. \quad (15)$$

The difference of the two output currents, $I_{d1} - I_{d2}$, is

$$I_{d1} - I_{d2} = \frac{I_e}{2I_2} I_{in}. \quad (16)$$

Replacing I_2 of Eq. (16) by I_2 of Eq. (10), we have the following expression:

$$I_{d1} - I_{d2} = \frac{I_e}{\sqrt{I_a I_o}} I_{in}. \quad (17)$$

When we use $I_{d1} - I_{d2}$ as the output current of the compressing circuit, $h(I_{out})$ becomes as follows:

$$h(I_{out}) = \frac{I_e}{\sqrt{I_a I_{out}}}. \quad (18)$$

where I_o is taken as I_{out} . Thus we can obtain the necessary form of gain which is given by Eq. (8).

In order to compress the input signal, the function $h(I_{out})$ must be

$$\frac{I_e}{\sqrt{I_a I_{out}}} < 1, \quad (19)$$

i.e.

$$I_e^2 < I_a (I_f + i_{out}), \quad (20)$$

where I_f and i_{out} are the output bias and signal current respectively.

3.2 Current-Mode Integrator

By combining the circuits of Figs. 2 and 3 to realize Eq. (8), we obtain the circuit shown in Fig. 5. To obtain the difference of two currents as shown in Eq. (17), we use two dividing circuits to which the same current I_2 is supplied through M7 and M6.

M12 in Fig. 5 is the expanding circuit having the gain of $f(V_2)$.

4 Simulation

Simulations of Fig. 5 were performed, based on a 0.5μ IC process ($V_{Tn} = 0.7V$, $V_{Tp} = -0.9$). Table 1 shows the aspect ratio of FETs. $V_{DD} = 3.3V$, $C = 1pF$,

Table 1: values of W/L

M1, M3 - M6, M8 - M10	1/1	M2, M11-12, M14	12.6/1
M7	6.3/1	M13, M15 - M17	2.1/1
M18	12.6/4		

$I_e = 10\mu A$, and $I_a = I_f = 100\mu A$. To guarantee the DC stability, 100% negative feedback is employed. This results in a first-order low-pass filter with a cutoff frequency of $\frac{1}{\pi} \sqrt{\frac{K}{I_a}} \frac{I_e}{C}$ which can be changed by controlling the bias currents I_a or I_e .

The small signal frequency responses are given in Fig. 6 in the cases of $I_e = 10\mu A$, $15\mu A$, and $20\mu A$. Theoretical value of the cutoff frequency for $I_e = 10\mu A$ is 2.6MHz, however the cutoff frequency of the simulated circuit is 2.35MHz. This error is caused by parasitic capacitance. However it may not be a serious problem because the cutoff frequency can easily be controlled by the bias current.

The transient analysis shows that the voltage swing of load capacitor C_L is suppressed within $30mV_{p-p}$ for the $10\mu A_{p-p}$ sinusoidal input.

Figure 7 shows the Total Harmonic Distortion (THD) versus input current amplitude of 1MHz sinusoidal input. We can see from Fig. 7 that THD of the proposed circuit is quite low over wide input current range.

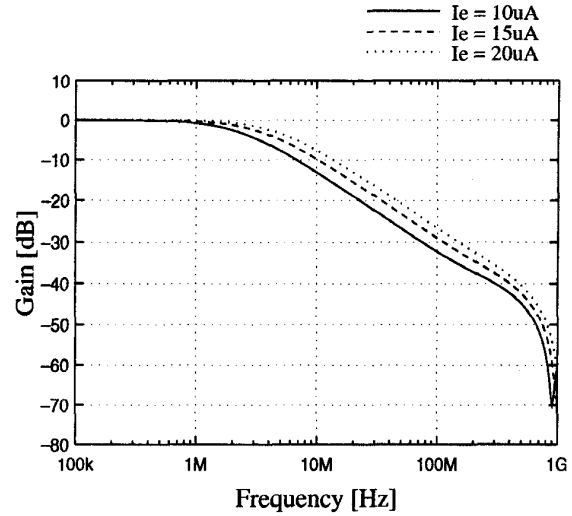


Figure 6: Frequency Responses

5 Conclusion

This paper has proposed CMOS companding current-mode integrator utilizing the MTL principle and the MOS FET square-law. The frequency responses of the filter employing the proposed integrator show quite good performance. Transient analysis indicates that THD becomes less than 1% with about $20\mu A_{p-p}$ sinusoidal input at 1MHz and a power supply voltage of 3.3V.

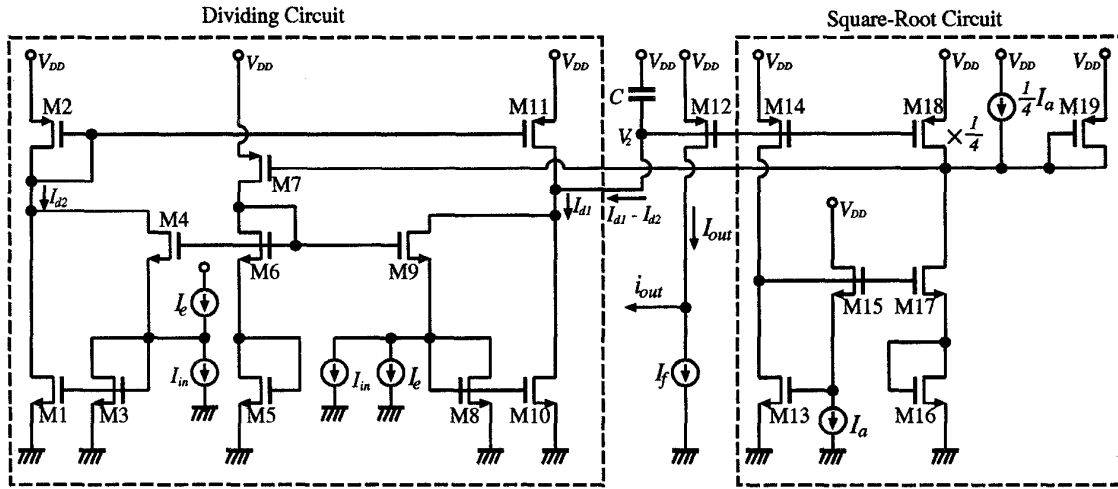


Figure 5: whole proposed circuit

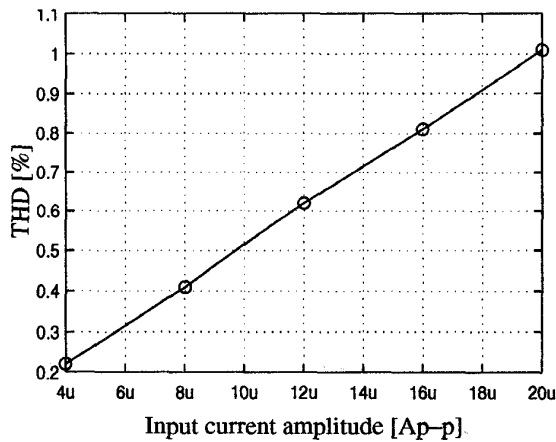


Figure 7: Total harmonic distortion

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